What is claimed is:

1. A data storage system comprising:

a plurality of pages, each of which includes a plurality of first memory cells, from which at least binary digital data can be read out a plurality of times without destruction of the data;

a circuit which receives a digital data output of at least one first page including the first memory cells, detects an error in at least one bit of data, and outputs information on a position of the error; and

a circuit which determines whether the bit of data where the error occurs is "1" or "0",

wherein when a result of the determination is "1" or "0", the first memory cell of the first page is selectively erased and error-corrected data is written therein.

2. The data storage system of claim 1, wherein the memory cells of the pages including the first memory cells are connected in common to one data selection line.

3. The data storage system of claim 1, wherein the memory cells of the pages including the

first memory cells constitute a memory cell block in which an erasure operation is carried out on the plurality of pages.

4. The data storage system of claim 1, wherein in the first memory cells, a plurality of reading operations generate a bit change to a writing state.

5. The data storage system of claim 1, wherein in the first memory cells, the reading operations generate a bit change to a writing state, and determination is selectively made when the bit of data where the error occurs is in an erased state before occurrence of the error.

6. The data storage system of claim 1, wherein the first memory cell further comprises a charge storage layer of insulating film for storing information based on the amount of charges stored in the charge storage layer.

7. The data storage system of claim 1, wherein the first memory cells comprise a memory cell having a NAND structure where current terminals

of the memory cells are serially connected.

8. The data storage system of claim 1, wherein the first memory cells comprise a memory cell having a virtual ground structure where the current terminals of the memory cells are connected in parallel.

9. The data storage system of claim 1, wherein if the number of information bits which enables recording of "1" or "0" from the external input/output section is n, and m is a natural number which satisfies $2^{m-1}-1<n\leq 2^{m}-m-1$, the number of memory cells of one page being at least (n+m).

10. The data storage system of claim 1, wherein for the first page including the first memory cells, all information bits can be read out from the external input/output section, and the first page can be read out when power starts to be supplied.

11. The data storage system of claim 1, wherein the first memory cells comprise a semiconductor memory cell transistor which stores at least

three digital values as a plurality of threshold values.

12. A data storage system comprising:

a plurality of pages, each of which includes a plurality of first memory cells, from which at least binary digital data can be read out a plurality of times without destruction of the data;

a circuit which receives a digital data output of at least one first page including the first memory cells, detects an error in at least one bit of data, and outputs information on a position of the error; and

a circuit which determines whether the bit of data where the error bit occurs is "1" or "0",

wherein when a result of the determination is "1" or "0", error-corrected data is written in the first memory cells of a page different from the first page.

13. A data storage system comprising:

a plurality of pages, each of which includes a plurality of first memory cells, from which at least binary digital data can be read out a plurality of times without

destruction of the data;

a plurality of pages including at least one page, each of which includes a plurality of second memory cells; and

a circuit which receives a digital data output of at least one first page including the first memory cells, and detects an error in at least one bit of data,

wherein a plurality of bits of position information on a position of the page where the error occurs is recorded in the second memory cells.

14. A data storage system comprising:

a plurality of pages, each of which includes a plurality of first memory cells, from which at least binary digital data can be read out a plurality of times without destruction of the data; and

a circuit which receives a digital data output of the first memory cells, and detects an error in at least one bit of data error,

wherein a bit change is generated when at least one of the first memory cells is in a held state of "1" or "0" and a reading operation is carried out a plurality of times;

the circuit is configured to have an external data output terminal to be capable of reading out all information bits for a first page of the first memory cells from an external input/output section and reading out the first page when power starts to be supplied; and

in the circuit, when the power is cut off or supplied, when a series of operations for reading out data of at least one page from the external data output terminal are repeated a plurality of times, the number of times of reading out information data identical to the information data written in the page is larger than the number of times of reading information data identical to the information data written in the page when the operation for continuously reading out the data of at least one page is carried out.

15. A data storage system comprising:

a memory macro including a memory cell array;

an error correction code circuit section connected to the memory macro; and

a temporary memory temporarily used for error correction of the memory cell array,

wherein the temporary memory is formed as a part of the memory cell array in the memory macro.

16. The data storage system of claim 3, wherein in the first memory cells, after data writing, a flag for indicating an end of the data writing is additionally written.

17. The data storage system of claim 3, wherein verify erasure is carried out in the memory cells of the pages including the first memory cells.

18. The data storage system of claim 6, wherein the charge storage layer comprises one of a silicon nitride film, a silicon oxynitride film and an alumina film.

19. The data storage system of claim 1, wherein if the number of information bits which enables recording of "1" or "0" from the external input/output section is n, and m and t are natural numbers which satisfy $2^{m-1}- t \times (m-1) 1<n\leq 2^{m}-t\times m-1$, the number of memory cells of one page being at least $(n+ t\times m)$.

20. The data storage system of claim 8, wherein in each of the first memory cells, a plurality of digital bits are stored in different positions of the charge storage layer.